ABSTRACT OF THE DISCLOSURE

The present invention provides a method and apparatus for design verification. The method comprises operating a device in the system in a first state, modifying at least one operational characteristic of the device to operate in a second state, and determining if an error condition occurs in the system in response to modifying the operational characteristic of the device. The apparatus comprises an interface and a verification module adapted to receive a control signal from the interface and to adjust an operating characteristic of the apparatus to exercise a system in a manner that is capable of revealing one or more error conditions in the system in response to receiving the control signal.